

10W+10W DUAL BRIDGE AMPLIFIER

1 FEATURES

- TECHNOLOGY BI20II
- WIDE SUPPLY VOLTAGE RANGE (6.5 - 18V)
- OUTPUT POWER 10+10W @ THD = 10%,
 $R_L = 8\Omega$, $V_{CC} = 13V$
- MINIMUM EXTERNAL COMPONENTS
 - NO SVR CAPACITOR
 - NO BOOTSTRAP
 - NO BOUCHEROT CELLS
 - INTERNALLY FIXED GAIN
- STAND-BY & MUTE FUNCTIONS
- SHORT CIRCUIT PROTECTION
- THERMAL OVERLOAD PROTECTION

Figure 1. Package



Table 1. Order Codes

| Part Number | Package |
|-------------|---------------------|
| TDA7297D | PowerSO20 (SLUG UP) |

2 DESCRIPTION

The TDA7297D is a dual bridge amplifier specially designed for Home Audio, Plasma TV, LCD TV applications.

Figure 2. TEST AND APPLICATION CIRCUIT

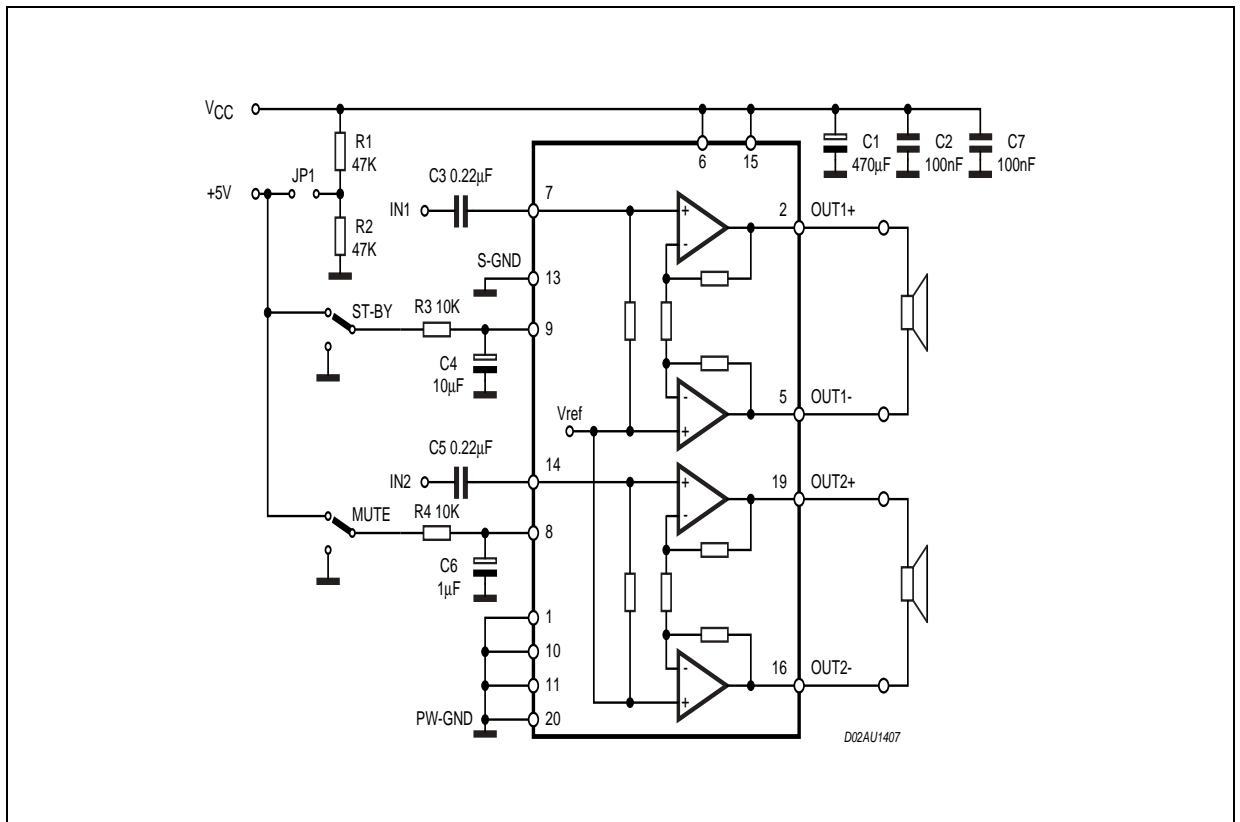


Table 2. Absolute Maximum Ratings

| Symbol | Parameter | Value | Unit |
|-----------------------------------|---------------------------------------------------|------------|------|
| V _s | Supply Voltage | 20 | V |
| I _O | Output Peak Current (internally limited) | 2 | A |
| P _{tot} | Total Power Dissipation (T _{amb} = 70°C) | 33 | W |
| T _{op} | Operating Temperature | 0 to 70 | °C |
| T _{stg} , T _j | Storage and Junction Temperature | -40 to 150 | °C |

Table 3. Thermal Data

| Symbol | Parameter | Value | Unit |
|------------------------|----------------------------------|-------|------|
| R _{th j-case} | Thermal Resistance Junction-case | 2.1 | °C/W |

Figure 3. PIN CONNECTION

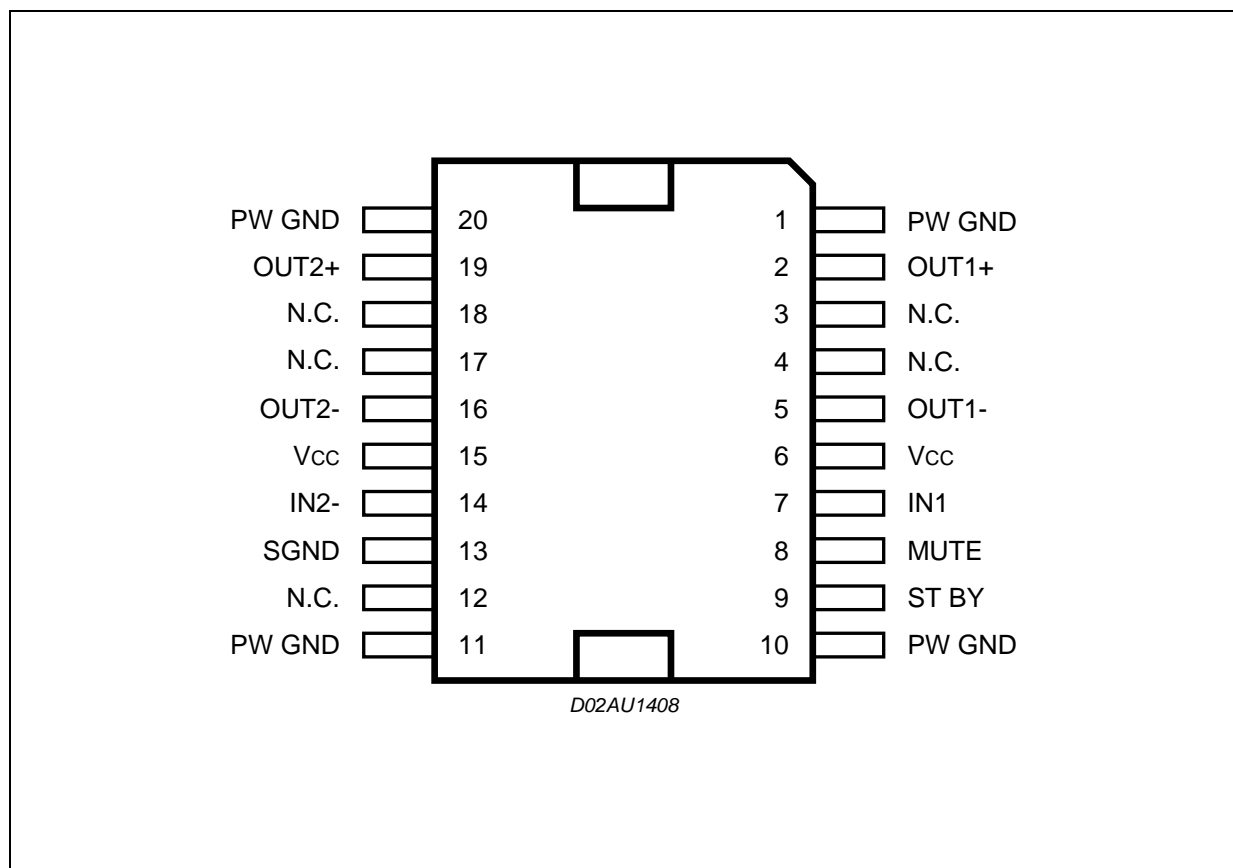


Table 4. Electrical Characteristics ($V_{CC} = 13V$, $R_L = 8\Omega$, $f = 1KHz$, $T_{amb} = 25^\circ C$ unless otherwise specified)

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|--------------|----------------------------|------------------------------------------------|------|------------|------|--------------------|
| V_{CC} | Supply Range | | 6.5 | | 18 | V |
| I_q | Total Quiescent Current | $R_L = \infty$ | | 50 | 65 | mA |
| V_{OS} | Output Offset Voltage | | | | 120 | mV |
| P_O | Output Power | THD 10% | 8.3 | 10 | | W |
| THD | Total Harmonic Distortion | $P_O = 1W$ | | 0.1 | 0.3 | % |
| | | $P_O = 0.1W$ to $5W$ $f = 100Hz$ to $15KHz$ | | | 1 | % |
| SVR | Supply Voltage Rejection | $f = 100Hz$, $V_R = 0.5V$ | 40 | 56 | | dB |
| CT | Crosstalk | | 46 | 60 | | dB |
| A_{MUTE} | Mute Attenuation | | 60 | 80 | | dB |
| T_w | Thermal Threshold | | | 150 | | $^\circ C$ |
| G_V | Closed Loop Voltage Gain | | 31 | 32 | 33 | dB |
| ΔG_V | Voltage Gain Matching | | | | 0.5 | dB |
| R_i | Input Resistance | | 25 | 30 | | $K\Omega$ |
| V_{TMUTE} | Mute Threshold | $V_o = -30dB$ | 2.3 | 2.9 | 4.1 | V |
| V_{TST-BY} | St-by Threshold | | 0.8 | 1.3 | 1.8 | V |
| I_{ST-BY} | St-by Current | | | | 100 | μA |
| e_N | Total Output Noise Voltage | A Curve $f = 20Hz$ to $20KHz$ | | 150 220 | 500 | μV μV |

3 APPLICATIVE SUGGESTIONS

STAND-BY AND MUTE FUNCTIONS

3.1 Microprocessor Application

In order to avoid annoying "Pop-Noise" during Turn-On/Off transients, it is necessary to guarantee the right St-by and mute signals sequence. It is quite simple to obtain this function using a microprocessor (Fig. 4 and 5).

At first St-by signal (from μP) goes high and the voltage across the St-by terminal (Pin 9) starts to increase exponentially. The external RC network is intended to turn-on slowly the biasing circuits of the amplifier, this to avoid "POP" and "CLICK" on the outputs.

When this voltage reaches the St-by threshold level, the amplifier is switched-on and the external capacitors in series to the input terminals (C1, C3) start to charge.

It's necessary to maintain the mute signal low until the capacitors are fully charged, this to avoid that the device goes in play mode causing a loud "Pop Noise" on the speakers.

A delay of 100-200ms between St-by and mute signals is suitable for a proper operation.

Figure 4. Microprocessor Application

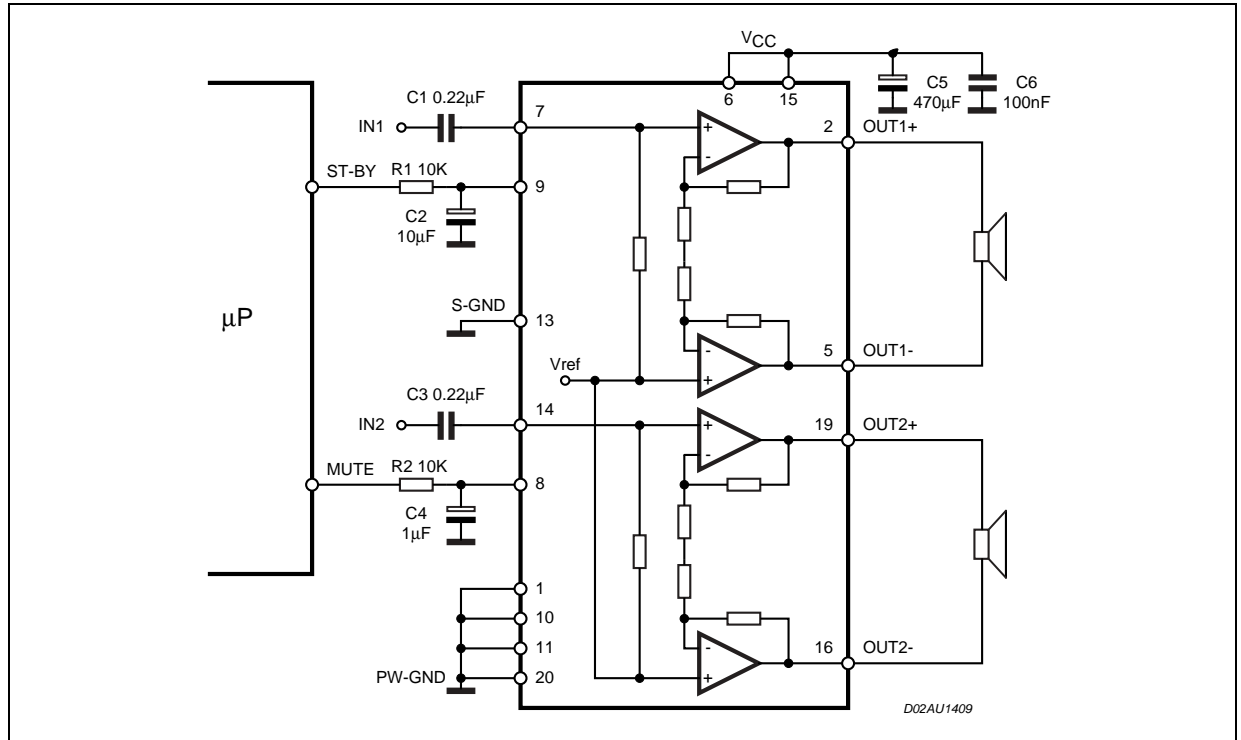


Figure 5. Microprocessor Driving Signals

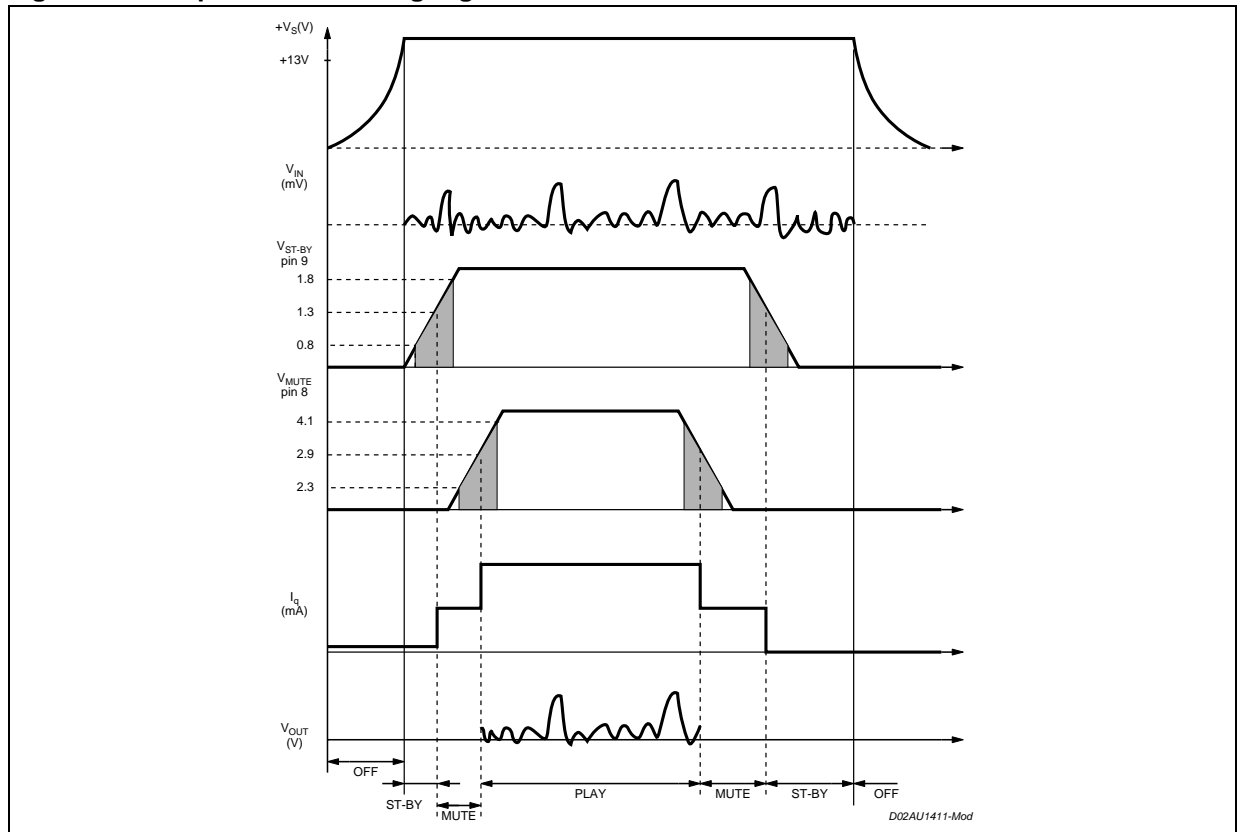


Figure 6. THD+N vs Output Power

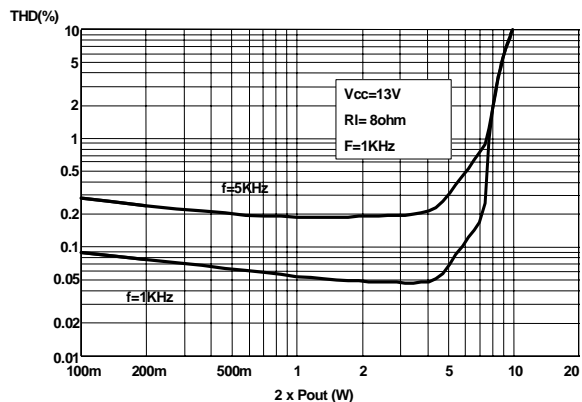


Figure 9. Frequency Response

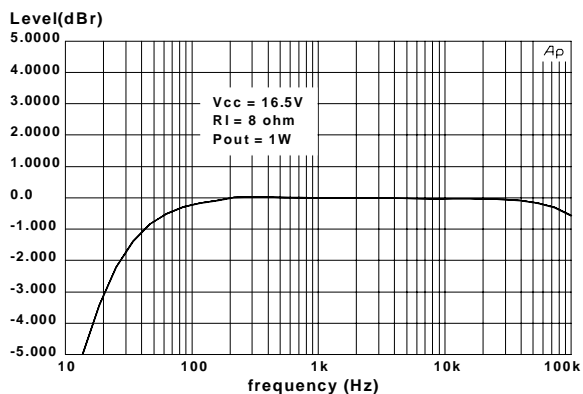


Figure 7. THD+N vs Output Power

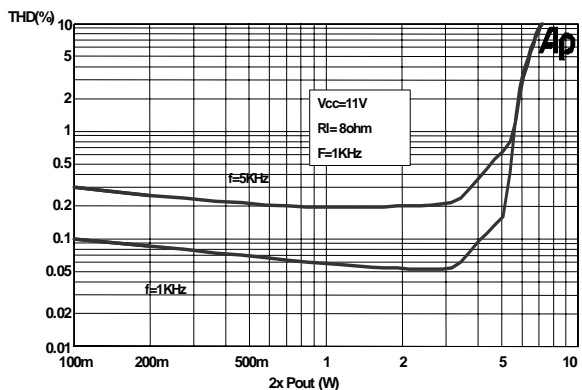


Figure 10. Output Power vs supply Voltage

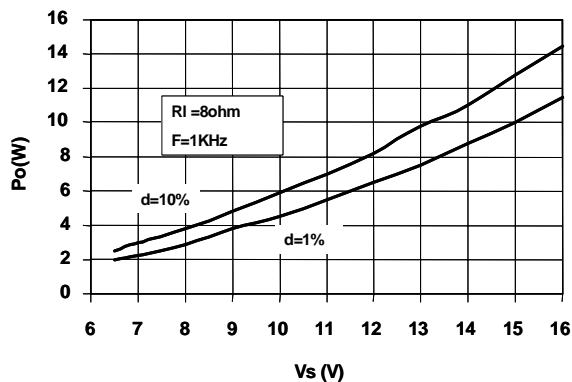


Figure 8. THD+N vs Frequency

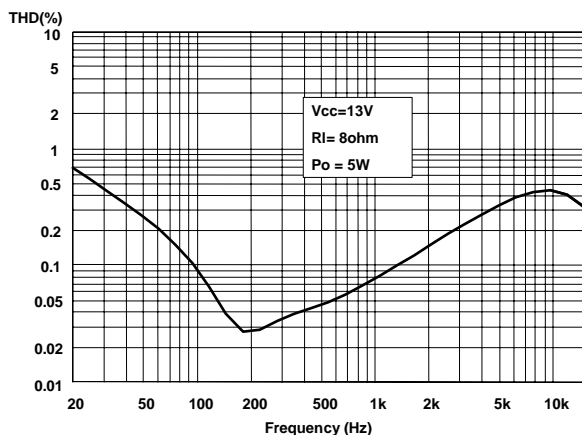


Figure 11. Power Dissipation vs Pout

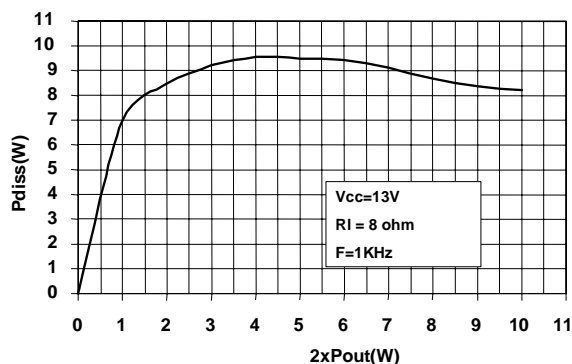


Figure 12. Mute Attenuation vs. Vpin 8t

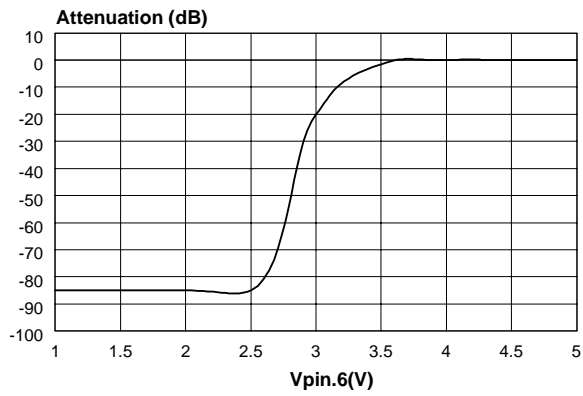


Figure 14. Quiescent Current vs. Supply Voltage

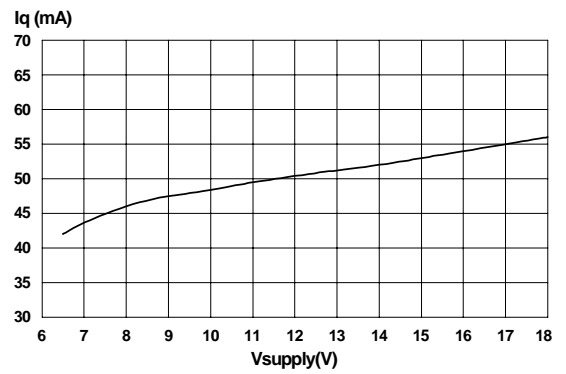


Figure 13. Standard-By Attenuation vs Vpin. 9

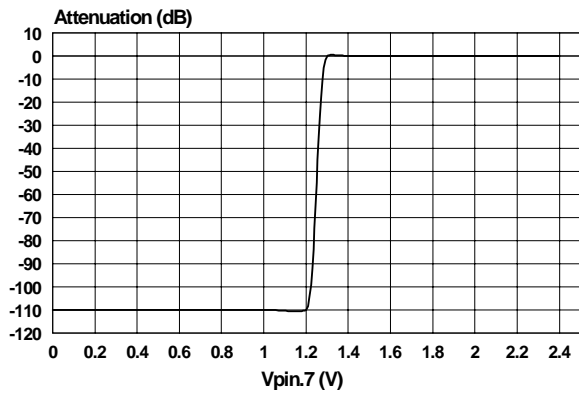


Figure 15. PC Board Component Layout

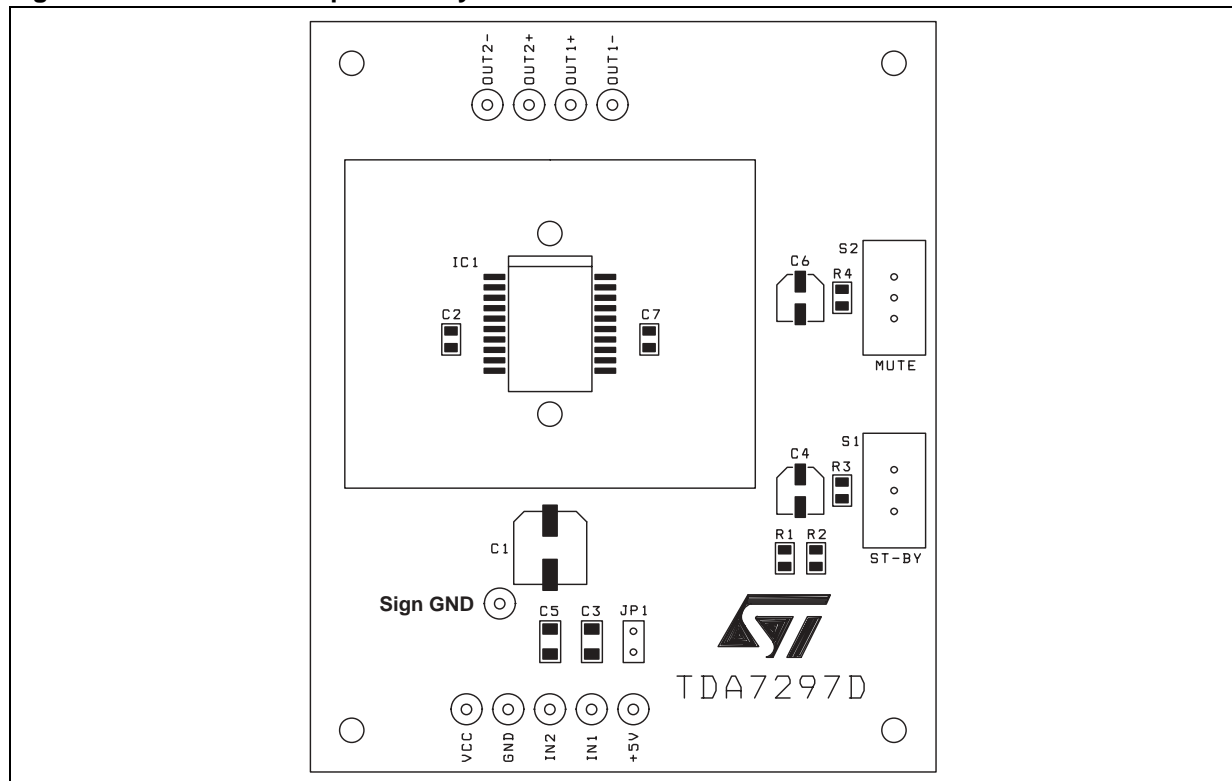


Figure 16. Evaluation Board Top Layer Layout

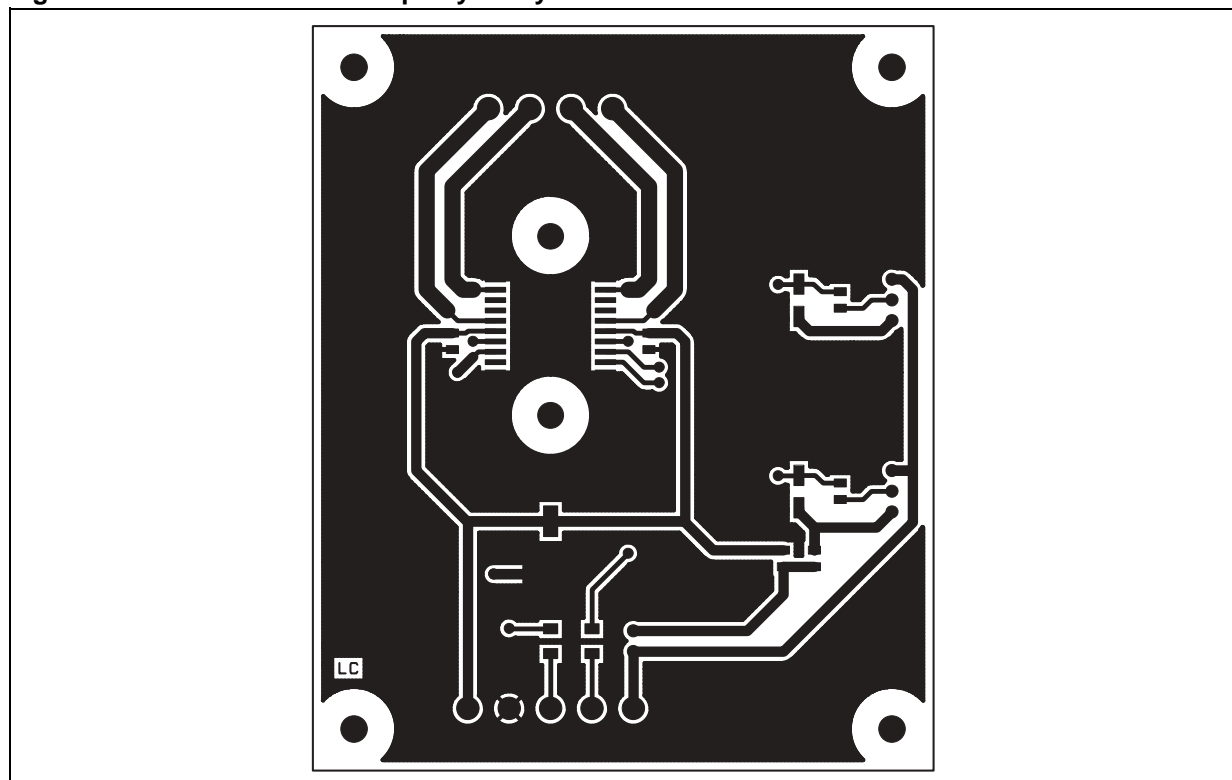


Figure 17. Evaluation Board Bottom Layer Layout

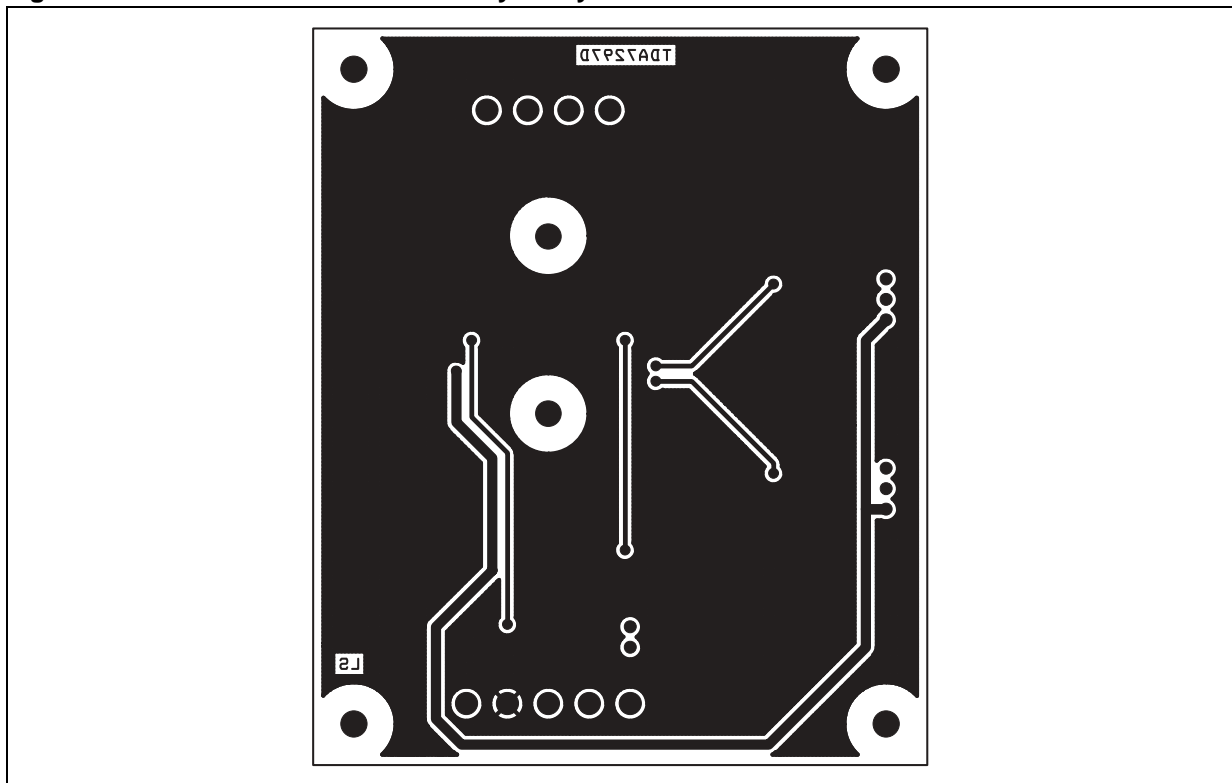
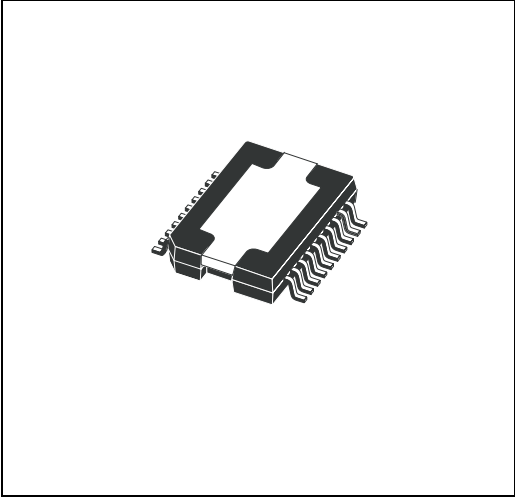


Figure 18. PowerSO20 (SLUG UP) Mechanical Data & Package Dimensions

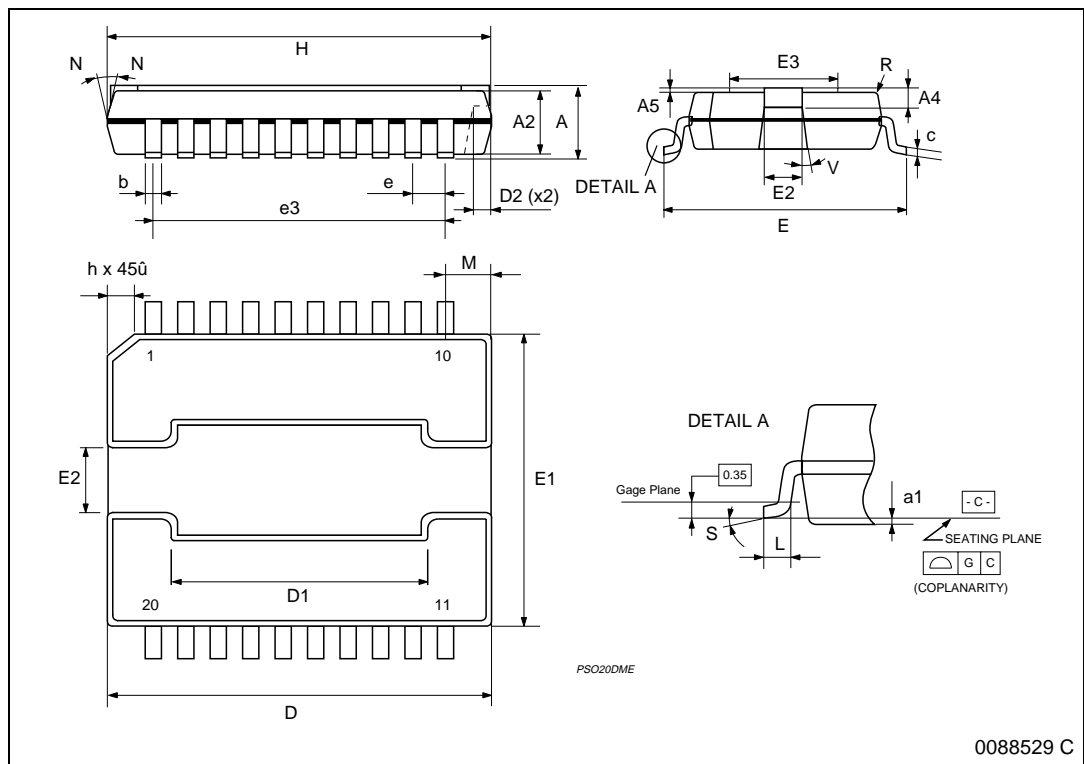
| DIM. | mm | | | inch | | |
|--------|---------------------------------------------|-------|--------|--------|-------|---------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | 3.25 | | 3.5 | 0.128 | | 0.138 |
| A2 | 3 | 3.15 | 3.3 | 0.118 | 0.124 | 0.130 |
| A4 | 0.8 | | 1 | 0.031 | | 0.039 |
| A5 | 0.15 | 0.2 | 0.25 | 0.006 | 0.008 | 0.010 |
| a1 | 0.030 | | -0.040 | 0.0012 | | -0.0016 |
| b | 0.4 | | 0.53 | 0.016 | | 0.021 |
| c | 0.23 | | 0.32 | 0.009 | | 0.012 |
| D (1) | 15.8 | | 16 | 0.622 | | 0.630 |
| D1 | 9.4 | | 9.8 | 0.370 | | 0.385 |
| D2 | | 1 | | | 0.039 | |
| E | 13.9 | | 14.5 | 0.547 | | 0.570 |
| E1 (1) | 10.9 | | 11.1 | 0.429 | | 0.437 |
| E2 | | | 2.9 | | | 0.114 |
| E3 | 5.8 | | 6.2 | 0.228 | | 0.244 |
| e | 1.12 | 1.27 | 1.42 | 0.044 | 0.050 | 0.056 |
| e3 | | 11.43 | | | 0.450 | |
| G | 0 | | 0.1 | 0 | | 0.004 |
| H | 15.5 | | 15.9 | 0.61 | | 0.625 |
| h | | | 1.1 | | | 0.043 |
| L | 0.8 | | 1.1 | 0.031 | | 0.043 |
| N | 10 _i (max) | | | | | |
| R | | 0.6 | | | 0.024 | |
| S | 0 _i (min.) 8 _j (max.) | | | | | |
| V | 5 _i (min.) 7 _j (max.) | | | | | |

OUTLINE AND MECHANICAL DATA



PowerSO20 (SLUG UP)

(1) $\varnothing D$ and $E1$ do not include mold flash or protrusions.
 - Mold flash or protrusions shall not exceed 0.15mm (0.006 \varnothing)
 - Critical dimensions: $\varnothing D$, $\varnothing A1$, $\varnothing e$ and $\varnothing V$.



0088529 C

Table 5. Revision History

| Date | Revision | Description of Changes |
|----------|----------|------------------------|
| May 2004 | 1 | First Issue |

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